

ABSTRACT OF THE DISCLOSURE

5 A method for improving the etch behavior of sidewall spacers in the fabrication of a CMOS device is disclosed. The etch rate of the material of the sidewall spacers depends on the implantation conditions. Thus, the etch rates are different for N-type and P-type transistors. To remove the sidewall spacers properly, the etch rates are altered by an implantation of ions, thereby modifying the structure of the material of the sidewall spacers and increasing the etch rate of the material. The increased etch rate leads to a shorter process time in the spacer removal process. Thus, the surrounding regions are less affected by the removal process and the device reliability and performance is improved.